# *Cascaded seven level inverter with reduced number of switches using level shifting PWM technique*

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***Abstract*— A multilevel inverter is a power electronic device that is used for high voltage and high power applications and has many advantages like, low switching stress, low total harmonic distortion (THD). Hence, the size and bulkiness of passive filters can be reduced. This paper proposes two new topologies of a 7-level cascaded multilevel inverter with reduced number of switches than that of conventional type which has 12 switches. The topologies consist of circuits with 9 switches and 7 switches for the same 7-level output. Therefore with less number of switches, there will be a reduction in gate drive circuitry and also very few switches will be conducting for specific intervals of time. The SPWM technique is implemented using multicarrier wave signals. Level Shifted triangular waves are used in comparison with sinusoidal reference to generate Sine PWM switching sequence. The number of level shifted triangular waves depends on the number of levels in the output. i.e. for n levels, n-1 number of carrier waves. This paper uses 1 KHz SPWM pulses with a modulation index of 0.8. The circuits are simulated using SPWM technique and the effect of the harmonic spectrum is analyzed. A comparison is made for the topologies with 9 switches and 7 switches and an effective reduction in THD has been observed for the circuits with less number of switches. The THD for 9 switches is 14% and the THD for 7 switches is 12.5%. The circuits are modeled and simulated with the help of MATLAB/SIMULINK.**

***Index Terms*— multilevel inverter; PWM Techniques; Total Harmonic Distortion** *(key words)*

## I. INTRODUCTION

The initial inverters developed were only of two levels. The technology got advanced and multi level inverters were developed which can produce a desired output of different voltage levels from many input DC voltage sources [1]. As the number of levels increase, the output attains near sinusoidal wave shape reducing the harmonics. The more the number of levels, the lesser is the harmonic content. Hence MLIs are becoming popular in applications where high voltage and high power are used. The disadvantage of MLI is that it involves many switches which require corresponding gate drive circuitry. This in turn increases the expenditure. Therefore the reduction in number of switches is essential. A conventional 7-level cascaded MLI requires 12 switches and the number of switches can be reduced to 9 [2] and 7. The respective circuits are simulated using MATLAB/SIMULINK and SPWM pulses are generated for the same using the phase opposition disposition method

## II. CONVENTIONAL 7-LEVEL CASCADED MLI

A stepped output voltage and current can be obtained in a cascaded MLI by cascading several H-bridge inverters. A single H-bridge serves the purpose of 3-level output $V_{dc}$, 0, $-V_{dc}$. On adding another H-bridge to the existing H-bridge, number of levels increase by two. Hence for a 7-level output, three H-bridge inverters are to be cascaded and it consists of 12 switches in total.

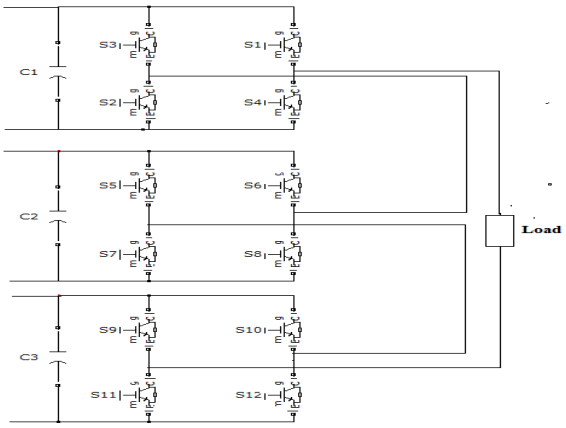


Fig.1 One leg of Typical 7- level cascaded multilevel inverter

## III. EXISTING 9-SWITCH TOPOLOGY

This topology consists of a series connected set of inverters which are capable of producing a stepped output [2]. No two switches in the same leg conduct at the same time so as to prevent short circuit across the voltage source. Each voltage source is $V_{dc}$ and thus we can get a maximum voltage $3V_{dc}$. We get 7-level output voltage having $V_{dc}$, $2V_{dc}$, $3V_{dc}$ in positive half cycle, zero level, $-V_{dc}$, $-2V_{dc}$, $-3V_{dc}$ in negative half cycle. H-bridge takes care of the positive and negative level voltages. Switches S1 and S2 serve for positive level. S3 and S4 serve for negative level.

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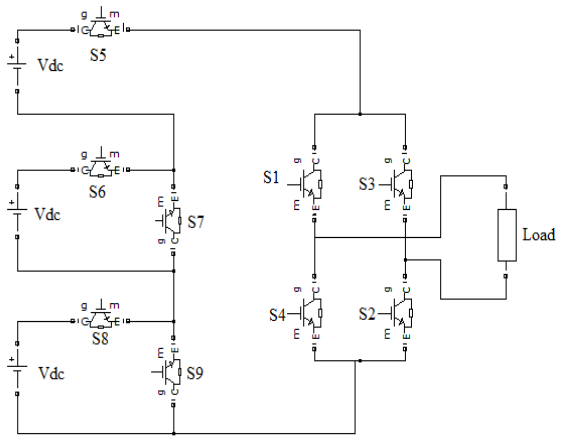


Fig.2 7-level using 9-switches topology

TABLE 1. SWITCHING STATES OF 9-SWITCH TOPOLOGY

| State | Switch S5 | Switch S6 | Switch S7 | Switch S8 | Switch S9 | Output Voltage |
|---|---|---|---|---|---|---|
| 1 | ON | OFF | ON | OFF | ON | Vdc |
| 2 | ON | ON | OFF | OFF | ON | Vdc+Vdc |
| 3 | ON | ON | OFF | ON | OFF | Vdc+Vdc+Vdc |

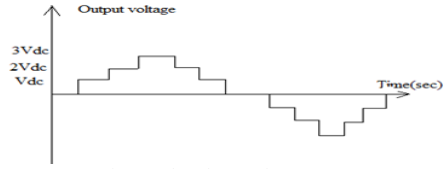


Fig. 3 7-level waveform

In order to reduce the harmonic distortion further, two more switches are reduced and thus 7-swicth topology is developed.

## IV. PROPOSED 7-SWITCH TOPOLOGY

Apart from the H-bridge, only one switch will be conducting at every instant and thus making the operation very simple. For example, we get output $V_{dc}$ only when S3 is conducting. The switching sequence for different voltage levels is shown below in the table. Each voltage source is $V_{dc}$.

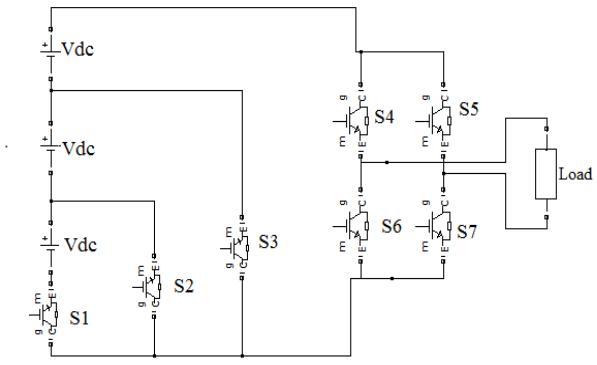


Fig.4 7-level using 7-switches topology

TABLE 2. SWITCHING STATES OF 7-SWITCH TOPOLOGY

| State | Switch S1 | Switch S2 | Switch S3 | Output voltage |
|---|---|---|---|---|
| 1 | OFF | OFF | ON | Vdc |
| 2 | OFF | ON | OFF | Vdc+Vdc |
| 3 | ON | OFF | OFF | Vdc+Vdc+Vdc |

## V. METHODOLOGY

There are two schemes of carried based modulation. They are phase shifting and level shifting methods. Phase shifting scheme produces higher amount of total harmonic distortion when compared to level shifting scheme. Therefore level shifting is taken into consideration.

Level shifting scheme is further divided into three schemes. In-phase disposition, phase opposition disposition, alternate phase opposition disposition [3]. While using level shifting scheme, an 'N' level inverter requires 'N-1' carrier waves. In-phase disposition involves all the carriers that are in phase. All the carrier waves above zero reference are in phase while the ones below zero are 180 degrees out of phase in case of phase opposition disposition. Each carrier is 180 degrees in phase difference with its neighboring carrier in alternate phase opposition disposition

This project is worked on phase opposition disposition scheme for the pulse generation for both 9 switch and 7 switch topologies. Positive pulses are generated when reference wave is greater than all the carrier waves. Zero level is produced when reference is greater than lower carriers and lesser than the upper carriers. Negative pulses are produced when reference is lesser than all the carrier waves as shown in fig.5

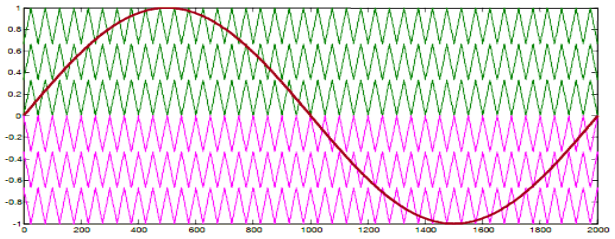

Fig.5 phase opposition disposition pwm

## VI. SIMULATION AND PULSE GENERATION RESULTS

The simulation is being done for the existing topology and the proposed topology by using nine and seven IGBT switches respectively. Simulations are done by using SPWM technique by comparing a sine wave and a triangular wave. Harmonic spectrum analysis also done through using FFT window in MATLAB/Simulink

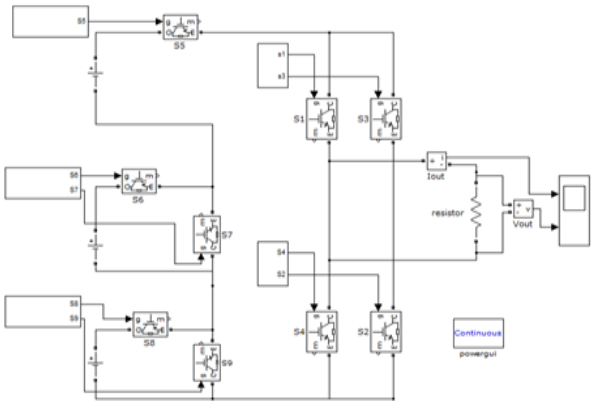


Fig.6 MATLAB/Simulink model of 7-level existing topology

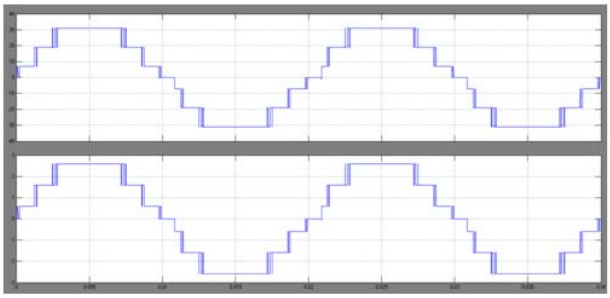

Fig.7 7-level inverter output using 9 switches

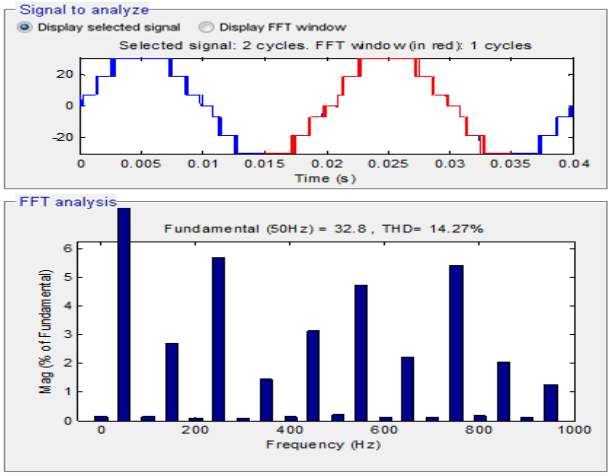


Fig. 8 FFT analysis of 7-level inverter using 9 switches

Fig.7 & Fig.8 Shows the output waveform of the 7-level inverter with nine switches which is being produced by SPWM technique [8] and it is done by comparing a triangular of 5 KHz with a sine wave of 50Hz. Although the Total Harmonic Distortion is very low, the 7$^{th}$ and the 13$^{th}$ order harmonics are high in this analysis.

Fig.9 Shows the MATLAB/simulink model of the proposed topology, in this model we are using only seven IGBT switches instead of nine in the existing topology .The pulses for the switches are being generated using SPWM technique and the FFT analysis window is being given in Fig.14

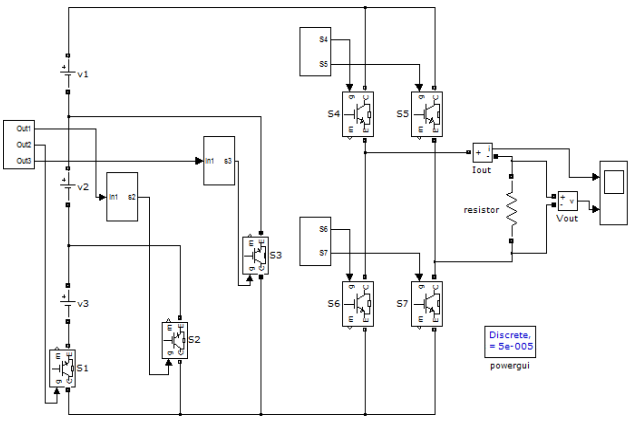


Fig.9 MATLAB/Simulink model of 7-level proposed topology

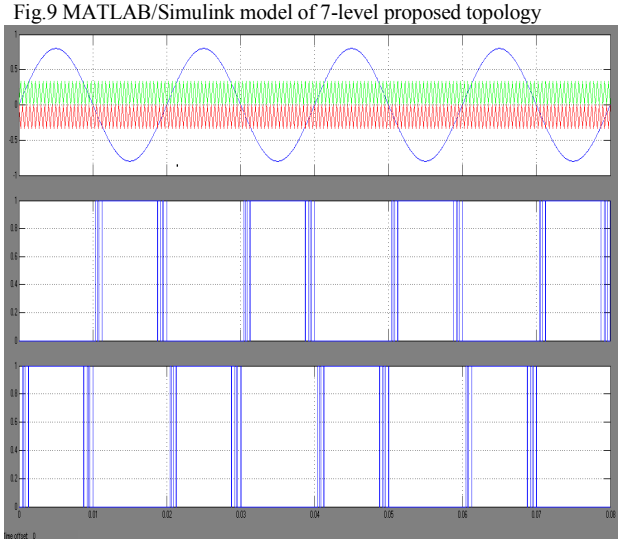

Fig. 10 Pulse generation using pod pwm method for S1 in proposed topology

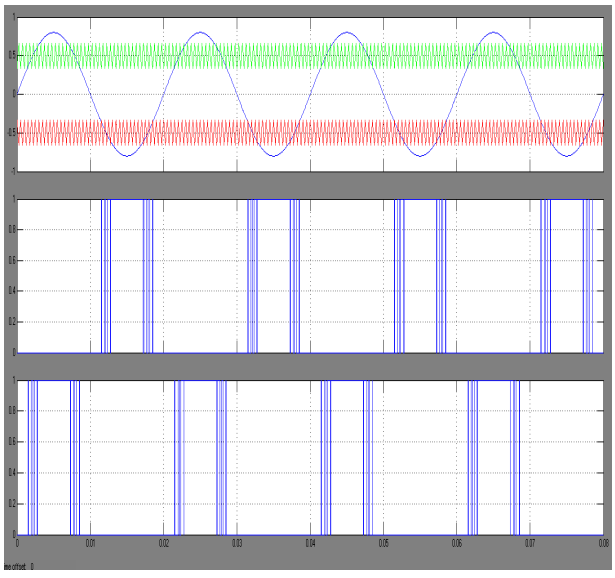

Fig. 11 Pulse generation using pod pwm method for S2in proposed topology

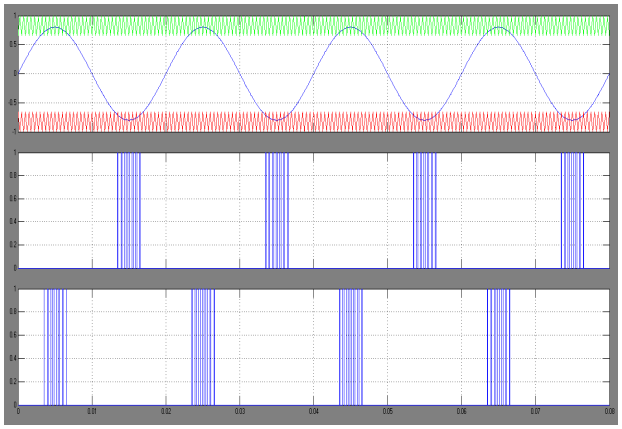

Fig. 12 Pulse generation using pod pwm method for S3 in proposed topology

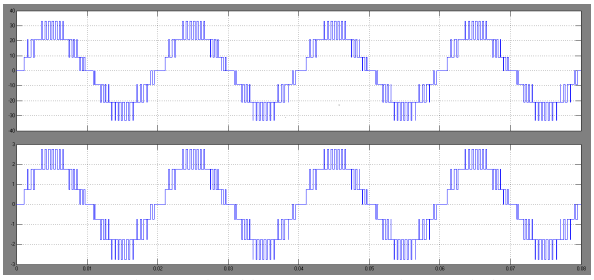

Fig. 13 7-level inverter output using 7 switches

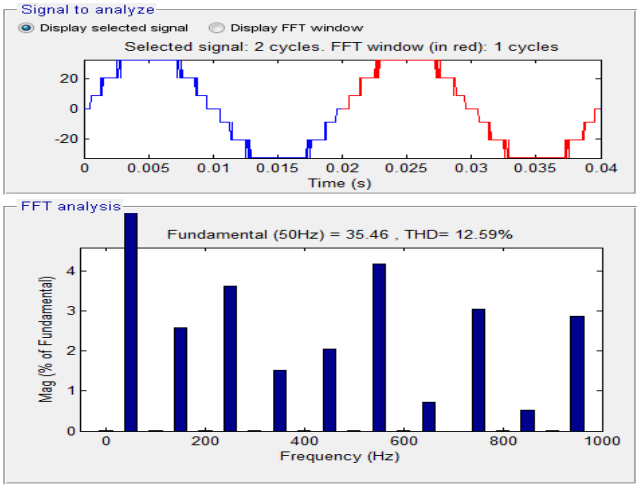


Fig. 14 FFT analysis of 7-level inverter using 7 switches

Fig.13& Fig.14 show the output voltage and the harmonic analysis of the proposed 7 level cascaded multilevel inverter using 7 switches. When compared to the existing method we will get more accurate sinusoidal output in the proposed method. The Total Harmonic Distortion is less in the proposed technology compared to existing topology the higher order harmonics are also very less compared to the existing technology.

The voltage stresses across switches is observed as s1>s2>s3. Here the stress on s1 is the greatest. Therefore ratings of respective IGBTs should be in the order s1>s2>s3

TABLE 3.COMPARISON OF VOLTAGE STRESS ACROSS SWITCHES

| Parameter | Switch S1 | Switch S2 | Switch S3 |
|---|---|---|---|
| Voltage stress | -18v | -6v | 6v |

TABLE 4.COMPARISON OF DIFFERENT MLI'S WITH PROPOSED 7-SWITCH TOPOLOGY

| | Capacitor clamped | Diode clamped | Cascaded | Proposed |
|---|---|---|---|---|
| No. of capacitors | 14 | 6 | - | - |
| No. of diodes | - | >=8 | - | - |
| No. of switches | 10 | 10 | 12 | 7 |

## VII. CONCLUSION

In this paper, a new topology with 7 switches and 9 switches are introduced and the same 7-level output is observed in either of the cases. Circuits are simulated using MATLAB/SIMULINK software and total harmonic distortions for both the circuits are obtained. It can be seen that there is a reduction in THD content for the 7-switch topology when compared to that of 9-switcht. Phase opposition disposition level shifting method is followed for the pulse generation for both the topologies.

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